[Para 17] The present invention, which provides a process for fabricating Si-containing resistors that are measured and adjusted post silicidation, will now be described in greater detail by referring to FIGS. 1A-1D that accompany the present application. In the accompanying drawings, like and/or corresponding elements are referred to by like reference numerals.

[Para 18] It is noted that the drawings of the present invention show a fragment of a semiconductor wafer or chip in which only one resistor device region is shown. Although the drawings show the presence of only a single resistor device region, the present process can be used in forming a plurality of resistors across different resistor device regions on the surface of a single semiconductor chip or wafer. Additionally, the process of the present invention can be integrated with any conventional CMOS, bipolar, or BiCMOS (bipolar and CMOS) processing scheme. Thus, other device regions including bipolar transistors and/or FETs can be formed to the periphery of the resistor device region shown in the drawings of the present application.

[Para 19] The following description provides details on one possible method that can be used in forming a resistor device. Specifically, the following description details the processing steps that are used in fabricating a precision polySi or polySiGe resistor device such as described in the U.S. Application mentioned in the Related Applications Section of the present application. Although this methodology is described in detail, the present invention also contemplates other methods, such as, for example, the method described in the Background Section of the present application, that can be used in forming a polySi or polySiGe resistor on a semiconductor substrate. The other methods are conventional and are known to those skilled in the art of semiconductor device manufacturing. Hence, the present invention is not limited to the specific processing steps described below in fabricating a polySi or polySiGe resistor on a substrate. Any processing scheme can be used and is contemplated herein.

Enter Brief description of the Drawing

[Para 20] Reference is first made to the initial structure 10 (i.e., a partial resistor) shown in FIG. 1A. The initial structure 10 includes semiconductor

DETAILED ACTION

Examiner's Amendment.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Please enter the following:

Brief Description of the Drawing:

FIGS. 1A-1D are pictorial representations (through cross sectional views) illustrating the basic processing steps that are employed in the present invention for fabricating a resistor.

FIGS. 2 is a graph showing the % shift of p+ polysilicon resistance Rs vs. rework rapid thermal anneal RTA time for various RTA temperatures after silicide processing.

FIGS. 3 is a graph showing the % delta p+ polysilicon resistance Rs vs. rework implant does for 750°C, 30 seconds and 650°C, 60 seconds rework RTA.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The central fax phone numbers for the organization where this application or proceeding is assigned are (571) 272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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